Dynamic Response of a-InGaZnO and Amorphous Silicon Thin-Film Transistors for Ultra-High Definition Active-Matrix Liquid Crystal Displays

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***Abstract*—The dynamic response of hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) and amorphous In-Ga-Zn-O (a-IGZO) TFT are compared. We study the storage capacitor ($C_{\rm st}$) charging characteristics by applying gate and data voltage waveforms corresponding to ultra-high definition (UHD) active-matrix liquid crystal displays (AM-LCDs). We show that the charging behavior of the a-Si:H TFT is insufficient for UHD AM-LCDs and that the a-IGZO TFT is capable of supporting at least 8 K×4 K display resolution at 480 Hz. The impact of $C_{\rm st}$ and gate voltage falling edge ($t_{\rm FE}$) on feedthrough voltage ($\Delta V_{\rm P}$) is investigated. Because of higher mobility of the a-IGZO TFT, it is possible to reduce $\Delta V_{\rm P}$ by mitigating channel charge redistribution with non-abrupt $t_{\rm FE}$. The a-IGZO TFT shows no drawbacks in terms of $\Delta V_{\rm P}$ when compared to the a-Si:H TFT. In addition, a larger $C_{\rm st}$ can be used in combination with the a-IGZO TFT to reduce $\Delta V_{\rm P}$ with minimal impact on its charging behavior. Gate overdrive operation is also evaluated for the a-IGZO TFT, which may improve charging characteristics with no adverse effects on $\Delta V_{\rm P}$. Our results show that the a-IGZO TFT is a suitable technology for UHD high-frame rate AM-LCDs.**

***Index Terms*—Active-matrix, a-IGZO, AM-LCD, amorphous silicon, dynamic response, falling edge, feedthrough voltage, flat-panel displays, overdrive, thin-film transistors (TFTs), ultra-high definition.**

I. Introduction

ULTRA-HIGH definition (UHD) information displays have resolutions of 4 K×2 K (3840×2160 pixels) or 8 K×4 K (7680×4320 pixels) and support frame rates of up to 120 Hz [1]. For 3D displays or motion blur reduction by image interpolation, frame rates of 240 Hz or higher are needed [2]. Improvements to display resolution and frame rate both correspond to shorter time margin available for each pixel to complete charging, thus placing stringent requirements on the dynamic response of thin-film transistor (TFT) backplane technology for active-matrix flat-panel displays (AM-FPDs). The dynamic response of the hydrogenated amorphous silicon (a-Si:H) TFT has been studied extensively in literature. The feedthrough voltage ($\Delta V_{\rm P}$), which results from gate-to-source overlap capacitance ($\rm C_{GS}$) and channel charge redistribution, is the main source of image flicker in active-matrix liquid crystal display (AM-LCD) operation and a key metric in TFT dynamic response [3]. Takabatake *et al.* reported a robust analytical model for $\Delta V_{\rm P}$ that is consistent with experimental values [4]. Kitazawa *et al.*investigated the impact of a-Si:H TFT device structural differences on $\Delta V_{\rm P}$ [5]. Aoki conducted a comprehensive study leading to an analytical model of a-Si:H TFT dynamic response including the liquid-crystal cell capacitance, and the model is verified by experimental data [6]. Lee *et al.* studied the dynamic response of a-Si:H TFT in the context of active-matrix organic light-emitting diode pixel circuit, and reported in detail $\Delta V_{\rm P}$ and charging time ($t_{\rm CH}$) for various TFT structures and waveform parameters [7].

The amorphous In–Ga–Zn–O (a-IGZO) TFT, because of its superior field-effect mobility ($\mu_{\rm FE}$) on the order of 10 $\rm cm^2/V\cdot s$ and good electrical stability, has emerged as a leading candidate for next-generation AM-FPD backplane technology [8]. Zhang *et al.* presented some preliminary results on the dynamic response of a-IGZO TFTs in terms of its storage capacitance ($C_{\rm st}$) and TFT dimension dependences [9]. Initial data suggest that a-IGZO TFTs have good dynamic characteristics when operated at very high frequencies. To date, however, there are still no peer-reviewed journal publications about a-IGZO TFT dynamic response.

In this paper, our objective is to evaluate and compare the dynamic response of a-Si:H and a-IGZO TFTs and their potential application to pixel circuits for UHD AM-LCDs. For this purpose, we have fabricated test circuits consisting of one TFT connected in series with a storage capacitor. Driving waveforms corresponding to UHD timing specifications are applied to the TFT and the resulting $C_{\rm st}$ charging characteristics are investigated. We study in detail the $\Delta V_{\rm P}$ voltage drop at $C_{\rm st}$ and its dependence on the gate voltage falling edge ($t_{\rm FE}$) for both a-Si:H and a-IGZO TFTs. Analytical equations from the literature are adopted to calculate $\Delta V_{\rm P}$ for various $t_{\rm FE}$ and $C_{\rm st}$ and compared to experimental observations. In addition, we also evaluate the

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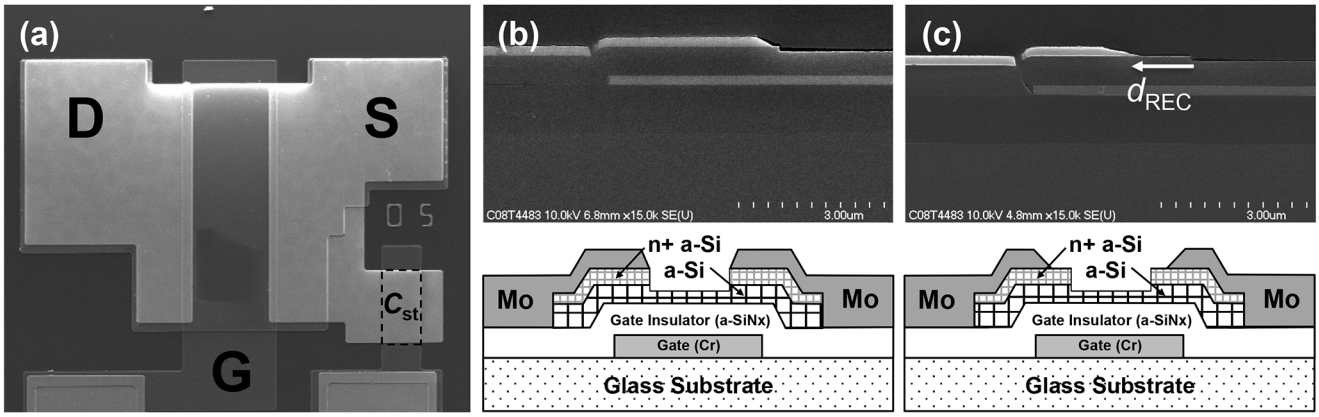

Fig. 1. (a) Top-view micrograph and (b) SEM image and cross-section diagram of the bottom-gate a-Si:H TFT used in this study. The SEM image and cross-section diagram of the a-Si:H TFT with the S/D-recess is shown in (c), where the recess length (d_{REC}) is 1 μm.

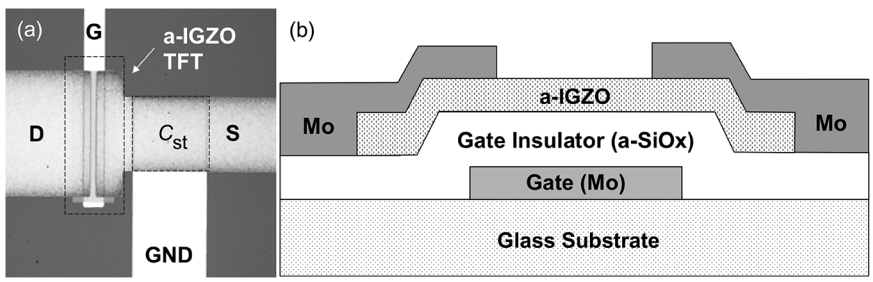

Fig. 2. (a) Top-view micrograph and (b) cross-sectional diagrams and SEM images of the bottom-gate a-IGZO TFT used in this study.

feasibility of overdriving the gate pulse voltage level of a-IGZO TFTs, which we expect should improve the dynamic response of a-IGZO TFTs with minimal negative impact.

II. Experimental

The fabrication of back channel etch (BCE)-type bottom-gate a-Si:H TFT follows the process described in Kuo *et al.* [10] and is briefly summarized here. The a-Si:H TFT has patterned chromium gate (200 nm) followed by amorphous silicon nitride (a-SiNx:H, 400 nm) and a-Si:H (170 nm), both deposited by PECVD. Near the gate insulator/semiconductor interface, deposition rates of PECVD a-Si:H and a-SiN_x:H are significantly reduced to promote higher film density and thus superior electrical properties. A 70-nm layer of phosphorous- doped n^+ a-Si:H is then deposited also by PECVD to act as source/drain (S/D) contact regions. The a-Si:H islands are then defined by dry etching using an SF_6:Cl_2:O_2:He gaseous mixture. The S/D electrodes are 200 nm of sputtered Mo and are wet-etched with a phosphorous-nitric-acetic acid mixture. The resulting gate-S/D metal overlap (OVLP) is 3 μm. During the S/D electrode definition, one set of TFTs ("S/D-recessed") is intentionally over-etched by 160 s such that the Mo S/D electrodes are recessed laterally from the channel region by 1 μm while the underlying n^+ a-Si:H layer is unmodified. Lastly, we dry-etched $(HBr{:}Cl_2)$ the n^+ a-Si:H completely and 70 nm of a-Si:H in the channel region. The a-Si:H TFT dimensions are width (W)/length $(L) = 57.5\ \mu\mathrm{m}/7.5\ \mu\mathrm{m}$. The patterned photoresist remained on top of the Mo electrodes throughout the S/D definition steps and is removed at the end. The storage capacitor of $C_{\mathrm{st}} = 0.19$ pF is fabricated at the same time as the TFT using the gate insulator layer as dielectric and is connected in series to the TFT source terminal. The a-Si:H TFT top-view micrograph and cross-section SEM images and diagrams illustrating the recess are shown in Fig. 1.

To fabricate the a-IGZO TFT, 100 nm of Mo is first deposited on a glass substrate (Corning Eagle or Asahi PD-200) using sputtering and the gate electrodes then defined using dry etching. The gate insulator is 200 nm of PECVD amorphous silicon oxide (a-SiO_x) deposited at 380 °C. The channel layer (50 nm) is then deposited by dc-sputtering an a-IGZO target of composition ratio In:Ga:Zn:O = 2:2:1:7. The a-IGZO active islands are defined using dilute oxalic acid (0.05 M) and then annealed in ambient air at 300 °C for 30 min on a hot plate. The gate vias are then opened using dry etching and subsequently 100 nm of Mo is sputtered during metallization. The S/D electrodes are defined using wet etching with 30% H_2O_2. The dimensions of the a-IGZO TFTs fabricated are $W/L = 74\ \mu\mathrm{m}/3\ \mu\mathrm{m}$ and OVLP $= 5\ \mu$m. The a-IGZO TFTs undergo one final annealing step of 300 °C for 30 min in ambient air. For the a-IGZO TFT, test circuits with three different storage capacitances are fabricated: $C_{\mathrm{st}} = 0.29$ pF, 0.65 pF, and 1.15 pF. The top-view micrograph and cross-section diagram of the a-IGZO TFT are shown in Fig. 2.

For the TFTs fabricated, we approximate C_{GS} in the area of gate-source overlap as two parallel plate capacitors connected in series:

$$C_{\mathrm{GS}} = W \times \mathrm{OVLP} \times \frac{1}{\frac{1}{C_{GI}} + \frac{1}{C_{act}}} \tag{1}$$

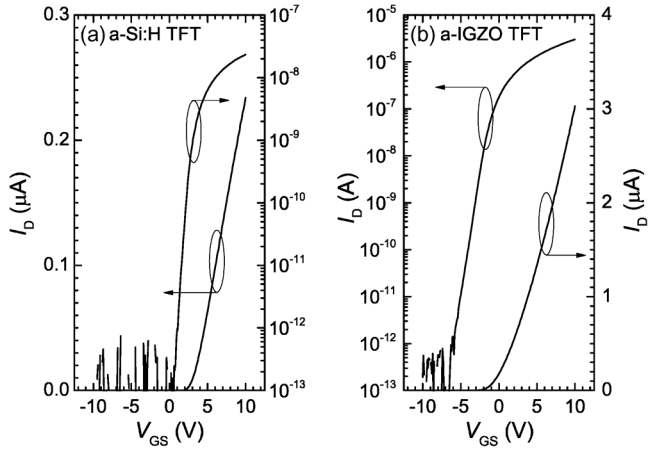

Fig. 3. The TFT transfer characteristics ($I_D - V_{GS}$) of the (a) a-Si:H (normal) and (b) a-IGZO TFTs. In both subfigures, $V_{DS} = 0.1$ V.

TABLE I
PARAMETERS OF THE THIN-FILM TRANSISTORS AND TEST CIRCUITS FABRICATED IN THIS SUDY

	a-Si:H	a-IGZO
W/L (μm/μm)	57.5/7.5	74/3
Gate-S/D Overlap (μm)	3	5
Gate Insulator Thickness (nm)	400	200
Active Layer Thickness (nm)	170	50
V_{th} (V)	3.1	0.3
μ_{FE} (cm^2/Vs)	0.29	9.1
C_{st} (pF)	0.19	0.29, 0.65, 1.15

where C_{GI} is the gate insulator capacitance per unit area and C_{act} is the active layer capacitance per unit area. Both C_{GI} and C_{act} can be calculated from the layer thickness and dielectric constant. Using (1), we calculate $C_{GS} = 0.021$ pF for normal a-Si:H TFTs and 0.06 pF for the a-IGZO TFTs. We expect C_{GS} to be lower than 0.021 pF for the S/D-recessed TFT, but not exactly reduced by 1/3 because the highly conductive n^+ regions are unmodified. The device transfer characteristics (I_D–V_{GS}) at drain-source voltage $V_{DS} = 0.1$ V are shown in Fig. 3(a) for normal a-Si:H TFT and Fig. 3(b) for a-IGZO TFT. The I_D–V_{GS} for S/D-recessed a-Si:H TFT is similar to the normal TFT and is omitted for clarity. The TFT device parameters are extracted from linear fits to the I_D–V_{GS} and are summarized together with device dimensions in Table I. We observe that the field-effect mobility of a-IGZO is much higher than a-Si:H, a well-established result in the literature [11]. In a-Si:H, conduction occurs through highly directional sp^3 orbitals, and carriers can be trapped within high-density localized states formed from bond angle fluctuations. In contrast, the conduction band minimum of a-IGZO is formed from the overlap of the large spherical s orbitals of the In^{3+} ions, which are relatively unaffected by structural disorder.

The setup for evaluating the dynamic response of a-Si:H and a-IGZO TFTs is as follows: a two-channel HP 8110A pulse generator is connected to the drain and gate electrodes of the test circuit, where the drain is the data signal and the gate is the select signal. A low-input capacitance (0.02 pF) and high-impedance (input leakage <10 fA) Picoprobe (18C-4-50-HV, GGB Industries) is used to measure the voltage of the storage capacitor C_{st} at the TFT source terminal. An Agilent MSO7104B oscilloscope is used to record the storage capacitor voltage measured by the Picoprobe with respect to time. Fig. 4(a) shows the schematic for the set-up used in this study. The waveforms applied to the gate and data lines are shown in Figs. 4(b) and 4(c) respectively. For each frame, two gate pulses of $V_{GH} = 18$ V are applied to the TFT gate electrode—one for set and another for reset. The low voltage of the gate waveform is $V_{GL} = -2$ V. The gate pulse width, indicated in Fig. 4(b) as the charging-time margin (t_{cm}), is the time available to charge/discharge C_{st} (for set/reset) in each pixel when the row lines are selected in active matrix operation. For a simple driving scheme without any charge sharing or pre-charging, t_{cm} is defined as [12]:

$$\text{Charging-time Margin}(t_{cm}) = \frac{1}{\text{Frame Rate} \times \text{Number of Row Lines}}. \quad (2)$$

In this study, we are most interested in the charging-time margins corresponding to UHD display specifications in [1]. Using (2), the t_{cm} are calculated based on these specifications and listed in Table II. The values in parentheses indicate t_{cm} rounded up to the next microsecond and are the values we used for the gate and data waveforms. For each frame, a single fixed pulse of data voltage $V_{DH} = 10$ V is applied to the drain terminal for set, after which the data voltage is returned to its low level $V_{DL} = 0$ V for reset. For the data voltage waveform, each set/reset period is defined to be $3 \times t_{cm}$. Each gate pulse arrives exactly $1 \times t_{cm}$ after the data voltage is applied/removed. The rising and falling edge time (t_{FE}) of the data and gate pulses are all 10 ns unless where specified. For falling edge values other than 10 ns, the corresponding rising edge is always 10% of that.

III. RESULTS AND DISCUSSION

A. Charging Characteristics of a-Si:H and a-IGZO TFTs for Ultra-High Definition AM-LCDs

The output voltages (V_{out}) at the source terminal of the a-Si:H or a-IGZO TFT as a function of time after applying the gate and data waveforms are shown in Fig. 5. In this figure, the gate and data waveforms are based on $t_{cm} = 16$ μs, which corresponds to Full HD 1080p resolution at 60 Hz—the current mainstream AM-LCD specification. In TFT dynamic response, one of the most important metrics is the storage capacitance charging behavior: incomplete charging directly causes the display gray-scale to deteriorate. Within this subsection, $C_{st} = 1.15$ pF is evaluated for the a-IGZO TFT to maximize the charging delay. In Fig. 5, both a-Si:H TFTs are able to charge C_{st} completely to $V_{DH} = 10$ V within 16 μs, but the charging curvature is clearly observable at the scale of the figure. In contrast, charging by the a-IGZO TFT appears almost instantaneous. From this figure, we can approximate the charging behavior as a simple RC process and extract the exponential-fit time constant (τ) for each device structure. The values of τ are 1.35 μs, 0.76 μs, and 0.08 μs for normal

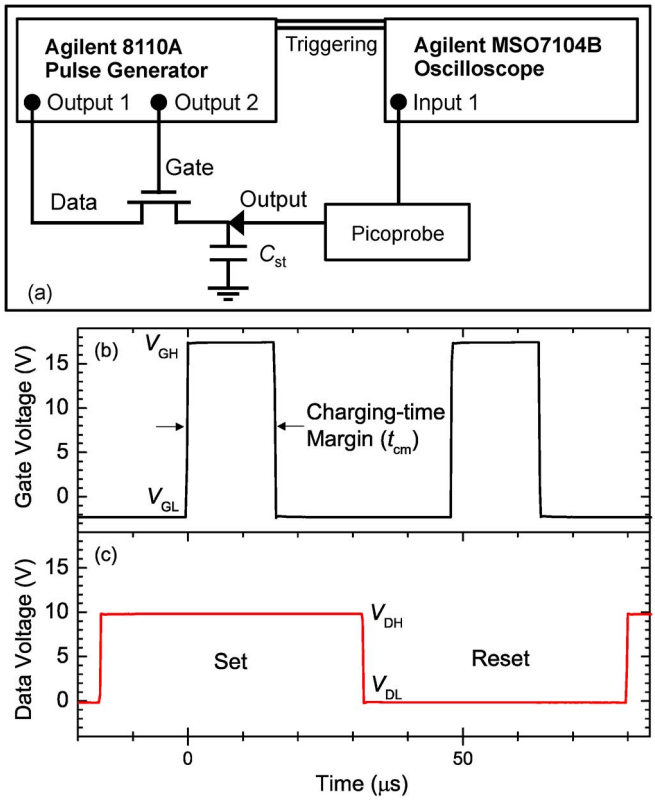

Fig. 4. (a) The schematic for the set-up used to evaluate the dynamic response of the one-TFT-one-capacitor test circuit. (b) The gate voltage applied is $V_{\rm GH} = 18$ V when charging/discharging and $V_{\rm GL} = -2$ V at all other times. The charging-time margin $t_{\rm cm}$ is the time available for the storage capacitor to completely charge/discharge. (c) The data voltage applied is $V_{\rm DH} = 10$ V for set and $V_{\rm DL} = 0$ V for reset. The set/reset duration is $3 \times t_{\rm cm}$. The falling edge of the waveforms is 10 ns except where specified.

TABLE II
THE CALCULATED CHANGING TIME MARGINS BASED ON AM-LCD RESOLUTION AND FRAME RATE SPECIFICATIONS

	Resolution		
	Full HD (1920×1080)	**4K UHD (3840×2160)**	**8K UHD (7680×4320)**
60 Hz	15.4 μs (16 μs)	7.7 μs (8 μs)	3.9 μs (4 μs)
120 Hz	7.7 μs (8 μs)	3.9 μs (4 μs)	1.9 μs (2 μs)
240 Hz	3.9 μs (4 μs)	1.9 μs (2 μs)	0.96 μs (1 μs)
480 Hz	1.9 μs (2 μs)	0.96 μs (1 μs)	0.48 μs (0.5 μs)

a-Si:H, S/D-recessed a-Si:H, and a-IGZO TFT, respectively. In the simple RC model, the TFT drain current $(I_{\rm D})$ supplies the charges to the capacitor

$$C_{\rm st}\frac{dV_{\rm out}}{dt} = I_D. \tag{3}$$

We can approximate $I_{\rm D}$ using the following simplified ideal MOSFET equation, which is appropriate for small $V_{\rm DS}$

$$I_D = \mu_{\rm FE} C_{GI}\frac{W}{L}(V_G - V_{\rm out} - V_{\rm th})(V_D - V_{\rm out}). \tag{4}$$

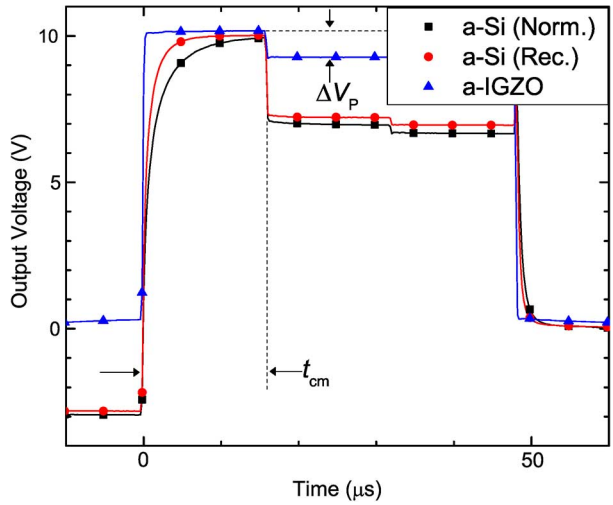

Fig. 5. The $V_{\rm out}$ measured at the source terminal of the a-Si:H or a-IGZO TFTs with the data and gate waveform applied. The feedthrough voltage $\Delta V_{\rm P}$ is the output voltage drop at the end of $t_{\rm cm}$ after the gate voltage is flipped from $V_{\rm GH}$ to $V_{\rm GL}$. Storage capacitances are 0.19 pF for a-Si:H TFTs and 1.15 pF for a-IGZO TFT.

Combining (3) and (4), and solving for time, the time required for charging $C_{\rm st}$ to a specific voltage $V_{\rm out}$ can be derived [7]

$$t_{\rm ch} = \frac{C_{\rm st}L}{\mu_{\rm FE}C_{GI}W}\frac{1}{(V_{\rm GH} - V_{\rm DH} - V_{\rm th})} \times \ln\frac{(V_{\rm GH} - V_{\rm out} - V_{\rm th})V_{\rm DH}}{(V_{\rm GH} - V_{\rm th})(V_{\rm DH} - V_{\rm out})}. \tag{5}$$

With regards to (5), τ approximately corresponds to the $t_{\rm ch}$ when $V_{\rm out} = 6.3$ V (0.63 $V_{\rm DH}$). We note that $t_{\rm ch}$ is directly proportional to $C_{\rm st}$ and inversely proportional to W/L, $C_{\rm GI}$, and $\mu_{\rm FE}$. To better compare the charging time for the different TFT dimensions and structures, we normalize τ and calculate $(\tau \times W \times C_{\rm GI})/(C_{\rm st} \times L)$ to be 0.828, 0.466, and 0.0308 (all in s/cm^2) for the normal a-Si:H, recessed a-Si:H, and a-IGZO TFT, respectively. It becomes obvious that the charging time of the a-IGZO TFT is at least an order of magnitude lower than that of any a-Si:H TFT.

To highlight the advantage of a-IGZO TFT over a-Si:H TFT in terms of charging characteristics, we apply gate and data waveforms based on the charging-time margins given in Table II, and show the resulting output voltages in Fig. 6 and Fig. 7. In Fig. 6(a), where $t_{\rm cm} = 16$ μs, the a-Si:H TFTs are capable of fully charging $C_{\rm st}$ within the allotted time. As $t_{\rm cm}$ is reduced to 8 μs and 4 μs in Fig. 6(b) and 6(c), the a-Si:H TFTs begin to struggle to charge the storage capacitor. In Fig. 6(d), where $t_{\rm cm} = 2$ μs represents the 8 K×4 K UHD AM-LCD at 120 Hz, the a-Si:H TFTs can only charge $C_{\rm st}$ to 7.2 V (normal) and 8.7 V (S/D-recessed). In real-world AM-LCD operation, gate and data bus-line RC delay may impose additional requirements for the charging-time margin [13], meaning that further degradations are expected for a-Si:H TFTs. In comparison, the simple BCE-type bottom-gate a-IGZO TFT is able to readily charge $C_{\rm st}$ to $V_{\rm DH} = 10$ V with ease for all four cases shown in Fig. 6. Charging of $C_{\rm st}$ by the a-IGZO TFT is shown in Fig. 7 for (a) $t_{\rm cm} = 1$ μs and (b) 0.5 μs, corresponding to 8 K ×

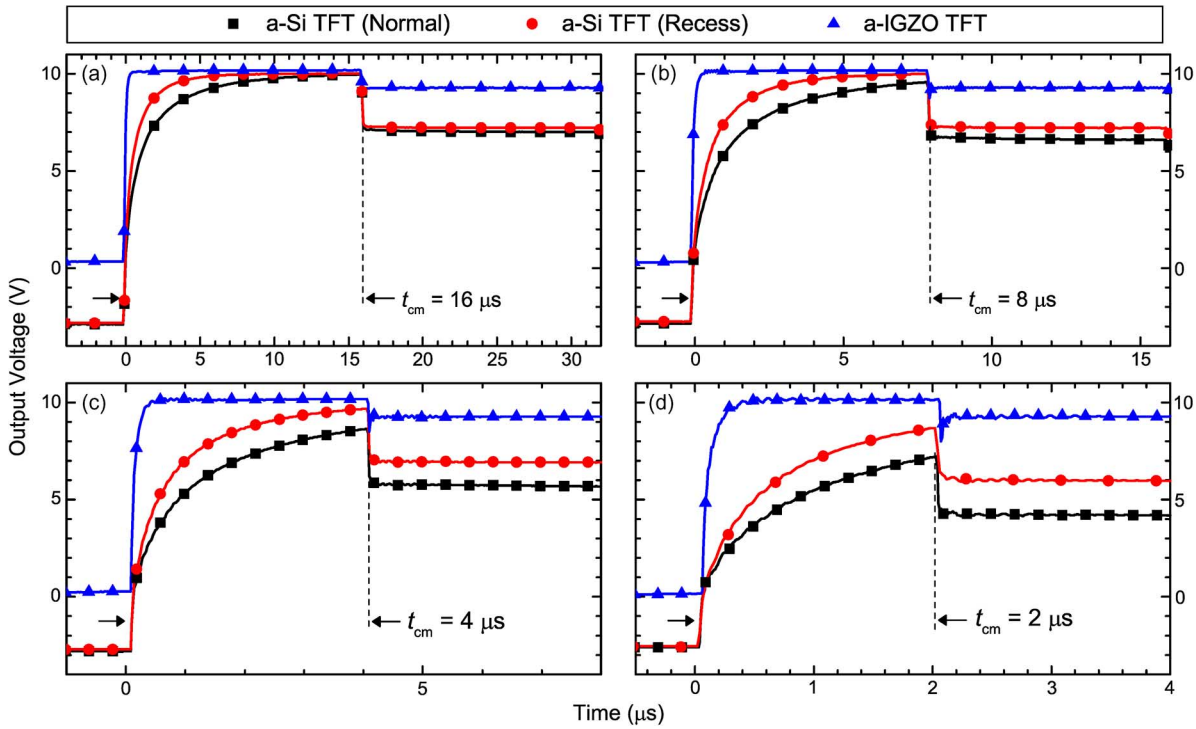

Fig. 6. Output voltage at the source terminal of the a-Si:H and a-IGZO TFTs after applying the gate and data voltage waveforms based on (a) $t_{\rm cm} = 16$ μs, (b) $t_{\rm cm} = 8$ μs, (c) $t_{\rm cm} = 4$ μs, (d) $t_{\rm cm} = 2$ μs, corresponding to the AM-LCD specifications in Table II. $C_{\rm st}$ is 1.15 pF for a-IGZO TFTs and 0.19 pF for a-Si:H TFTs.

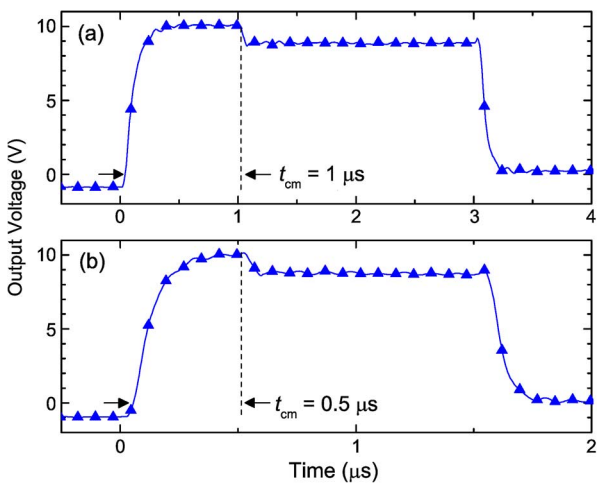

Fig. 7. The output voltage at the source terminal of the a-IGZO TFTs after applying the gate and data voltage waveforms based on (a) $t_{\rm cm} = 1$ μs and (b) $t_{\rm cm} = 0.5$ μs corresponding to 8 K $\times$ 4 K resolution at 240 and 480 Hz. For this figure, $C_{\rm st} = 1.15$ pF.

4 K resolution at 240 and 480 Hz, and the $C_{\rm st}$ is fully charged to $V_{\rm DH}$ before the end of $t_{\rm cm}$.

B. Feedthrough Voltage of a-Si:H and a-IGZO TFTs

The feedthrough voltage $\Delta V_{\rm P}$ shown in Fig. 5 is the voltage drop at $C_{\rm st}$ after the gate voltage $V_{\rm G}$ flips from $V_{\rm GH}$ to $V_{\rm GL}$. It was originally observed as clock feedthrough in CMOS switched-capacitor circuits, affecting its high-frequency accuracy [14]. In AM-LCD operation, $\Delta V_{\rm P}$ at the pixel electrode primarily manifests itself as image flickering [3]. Takabatake *et al.* developed a series of equations describing $\Delta V_{\rm P}$ [4], which we briefly summarize below.

There are two primary contributions to $\Delta V_{\rm P}$: channel charge redistribution when $V_{\rm G}$ is reduced from $V_{\rm GH}$ to $V_{\rm th} + V_{\rm DH}$, and capacitance feedthrough from $C_{\rm GS}$ to $C_{\rm st}$ when $V_{\rm G}$ is reduced from $V_{\rm th} + V_{\rm DH}$ to $V_{\rm GL}$. Channel charge redistribution occurs when the TFT switches from its ON- to OFF-state and the accumulated channel charge ($Q_{\rm ch}$) is released towards the source and drain terminals. We can estimate $Q_{\rm ch}$ in the area of overlap (A) between the gate electrode and the active layer with the equation

$$Q_{\rm ch} = C_{GI} A (V_{\rm GH} - V_{\rm th} - V_{\rm DH}). \tag{6}$$

In our TFTs, we calculate the overlap area as $A = W \times (L + 2{\rm OVLP})$. When $V_{\rm G} = V_{\rm th} + V_{\rm DH}$, the TFT is turned off and half of any $Q_{\rm ch}$ in the channel is redistributed onto $C_{\rm st}$

$$\Delta V_{P,CR} = \alpha \frac{Q_{\rm ch}}{C_{\rm st}} = \alpha \frac{C_{GI} A (V_{\rm GH} - V_{\rm th} - V_{\rm DH})}{C_{\rm st}} \tag{7}$$

where α is a constant factor related to the gate voltage falling edge. The capacitance feedthrough component of $\Delta V_{\rm P}$ can be calculated from

$$\Delta V_{P,F} = \frac{C_{\rm GS}}{C_{\rm GS} + C_{\rm st}} (V_{\rm th} + V_{\rm DH} - V_{GL}). \tag{8}$$

In (8), capacitance feedthrough primarily depends on the ratio between $C_{\rm GS}$ and $C_{\rm st}$. Overlap capacitance $C_{\rm GS}$ can be eliminated through the use of a self-aligned structure [15]–[18], but is difficult to avoid in the commonly used bottom-gate staggered

structure such as the TFTs in this study. The total $\Delta V_{\rm P}$ is a sum of (7) and (8)

$$\begin{aligned}\Delta V_P &= \Delta V_{P,F} + \Delta V_{P,CR} \\ &= \frac{C_{\rm GS}}{C_{\rm GS}+C_{\rm st}}(V_{\rm th}+V_{\rm DH}-V_{GL}) \\ &\quad + \alpha\frac{C_{GI}A(V_{\rm GH}-V_{\rm th}-V_{\rm DH})}{C_{\rm st}}. \end{aligned} \tag{9}$$

The factor α ranges from 0 to 0.5, depending on how fast the drop from $V_{\rm GH}$ to $V_{\rm DH}+V_{\rm th}$ is. For a very short $t_{\rm FE}$, the TFT is turned off so abruptly that no charges can be released through the drain terminal while $V_{\rm G}$ is reduced from $V_{\rm GH}$ to $V_{\rm th}+V_{\rm DH}$. In this upper limit of $\alpha = 0.5$, $t_{\rm FE}$ satisfies the condition:

$$t_{\rm FE} \ll \frac{L^2}{\mu_{\rm FE}\cdot\Delta V_{\rm P,CR}}. \tag{10}$$

The right-hand side of (10) is the channel transit time for accumulated charges. For longer $t_{\rm FE}$, α decreases until it approaches the lower limit of $\alpha = 0$. In this lower limit, $t_{\rm FE}$ is much slower than channel transit time of charge carriers

$$t_{\rm FE} \gg \frac{L^2}{\mu_{\rm FE}\cdot\Delta V_{\rm P,CR}}. \tag{11}$$

In this case, most, if not all, of $Q_{\rm ch}$ can be released through the drain terminal while $V_{\rm G}$ is reduced from $V_{\rm GH}$ to $V_{\rm th}+V_{\rm DH}$. Contribution from $\Delta V_{\rm P,CR}$ then becomes negligible ($\alpha \approx 0$) and the total feedthrough voltage is simply

$$\Delta V_P = \Delta V_{P,F} = \frac{C_{\rm GS}}{C_{\rm GS}+C_{\rm st}}(V_{\rm th}+V_{\rm DH}-V_{GL}). \tag{12}$$

We note that according (12), in the case of large $t_{\rm FE}$, $\Delta V_{\rm P}$ does not depend on $V_{\rm GH}$. We can experimentally verify this by comparing the $V_{\rm GH}$ dependence of $\Delta V_{\rm P}$ for slow and fast $t_{\rm FE}$. The output voltage of the a-IGZO TFT test circuit is shown in Fig. 8, where the falling edge of the gate pulse is (a) $t_{\rm FE} = 10$ ns and (b) $t_{\rm FE} = 10$ μs. In Fig. 8(c), $\Delta V_{\rm P}$ corresponding to different $V_{\rm GH}$ are extracted for $t_{\rm FE} = 10$ μs, 1 μs, and 10 ns. We first calculate the $\Delta V_{\rm P}$ for various $V_{\rm GH}$ using (9) with $\alpha = 0.5$ and we find that the generated values are much larger than the experimental data for $t_{\rm FE} = 10$ ns. This means that the actual fast-$t_{\rm FE}$ limit for a-IGZO TFTs is much smaller than 10 ns. Using (10), we calculate the channel transit time of the a-IGZO TFT to be 7.2 ns. This is consistent with what we observe in Fig. 8(c) in that (10) is not satisfied because channel transit time and $t_{\rm FE}$ are on the same order of magnitude and thus $\alpha < 0.5$. For $t_{\rm FE} = 10$ ns, we find that (9) with $\alpha = 0.32$ models the experimental data quite well. In the same figure, $\Delta V_{\rm P}$ appears to be independent of $V_{\rm GH}$ for $t_{\rm FE} = 10$ μs and can be well described by (12). This means that $t_{\rm FE} = 10$ μs, which is three orders of magnitude larger than the channel transit time, can be considered as the slow-$t_{\rm FE}$ limit and (11) is satisfied.

In Fig. 9, we compare the impact of $t_{\rm FE}$ on the $\Delta V_{\rm P}$ of (a) normal a-Si:H and (b) a-IGZO TFT by varying $t_{\rm FE}$ from 10 ns to 10 μs. The extracted $\Delta V_{\rm P}$ at various $t_{\rm FE}$ are shown in Fig. 9(c) for normal a-Si:H and a-IGZO TFTs. For a change of three orders of magnitude in $t_{\rm FE}$, $\Delta V_{\rm P}$ decreases by only 0.3 V for the a-Si:H TFT. Upon inspection, $\Delta V_{\rm P}$ appears to be almost unchanged from $t_{\rm FE} = 10$ ns to 1 μs. In contrast, $\Delta V_{\rm P}$

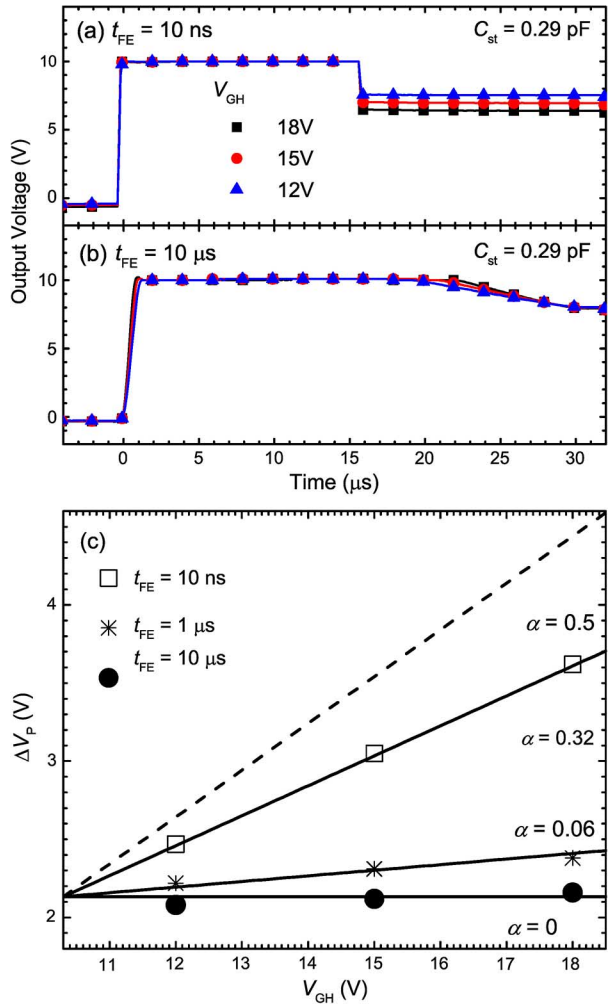

Fig. 8. The output voltage of the a-IGZO TFT test circuit for waveforms with $V_{\rm GH}$ varied from 18 to 12 V for (a) $t_{\rm FE} = 10$ ns and (b) $t_{\rm FE} = 10$ μs. The storage capacitance tested in this figure is 0.29 pF. In (c), the $\Delta V_{\rm P}$ extracted for $t_{\rm FE} = 10$ ns (empty squares), 1 μs (solid circles), and 10 μs (asterisks) are shown. The calculated $\Delta V_{\rm P}$ values are also shown in the figure for $\alpha = 0$ to 0.5.

decreases by 1.6 V for the a-IGZO TFT over the same range of $t_{\rm FE}$ values. This significant difference is primarily due the fact that the $\mu_{\rm FE}$ of a-IGZO is more than an order of magnitude larger than that of a-Si:H, which would allow (11) to be fulfilled at a lower $t_{\rm FE}$. We calculate the channel transit time to be 1.2 μs for a-Si:H TFTs and it is shown in Fig. 9(c) together with that for a-IGZO TFTs. Our experimental observations are consistent with these two values in that for a-Si:H TFTs, $\Delta V_{\rm P}$ remains almost constant for $t_{\rm FE} < 1$ μs. For a-IGZO TFTs, $\Delta V_{\rm P}$ is seen to be decreasing for all $t_{\rm FE}$ because no $t_{\rm FE}$ faster than 10 ns is tested in this study. An implication of Fig. 9 is that for the a-IGZO TFT, because of the shorter channel transit time, it may be possible to reduce $\Delta V_{\rm P}$ by controlling the $t_{\rm FE}$, while the same is difficult to realize for a-Si:H TFTs. The $\Delta V_{\rm P}$ for the S/D-recessed a-Si:H TFT (not shown) is similar to the normal a-Si:H TFT curve shifted downward with the overall trend remaining the same. We have omitted some of the experimental data for the S/D-recessed a-Si:H TFT in this section because only marginal improvements to $\Delta V_{\rm P}$ (<10%) have been observed. This is most likely due to the fact that the n^+-doped

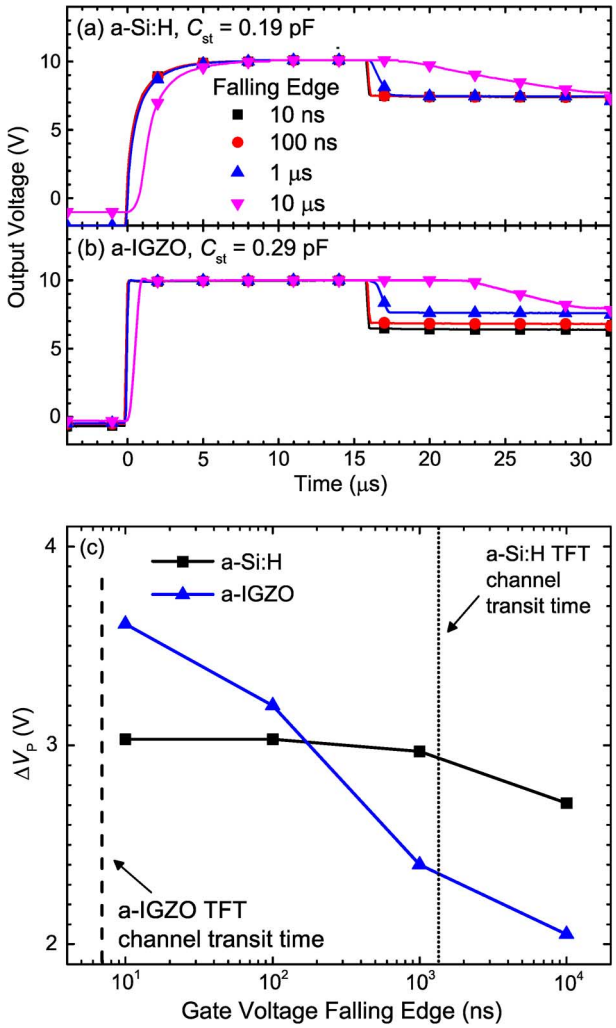

Fig. 9. The $V_{\rm out}$ of the (a) a-Si:H and (b) a-IGZO TFT test circuits for waveforms with $t_{\rm FE}$ varied from 10 ns to 10 μs. The $C_{\rm st}$ evaluated in this figure is 0.19 pF and 0.29 pF for the a-IGZO and a-Si:H TFTs, respectively. The $\Delta V_{\rm P}$ are extracted from (a) and (b) and shown in (c). Using (10), the channel transit time is calculated and denoted (c) as dashed line and dotted line for the a-IGZO and a-Si:H TFTs.

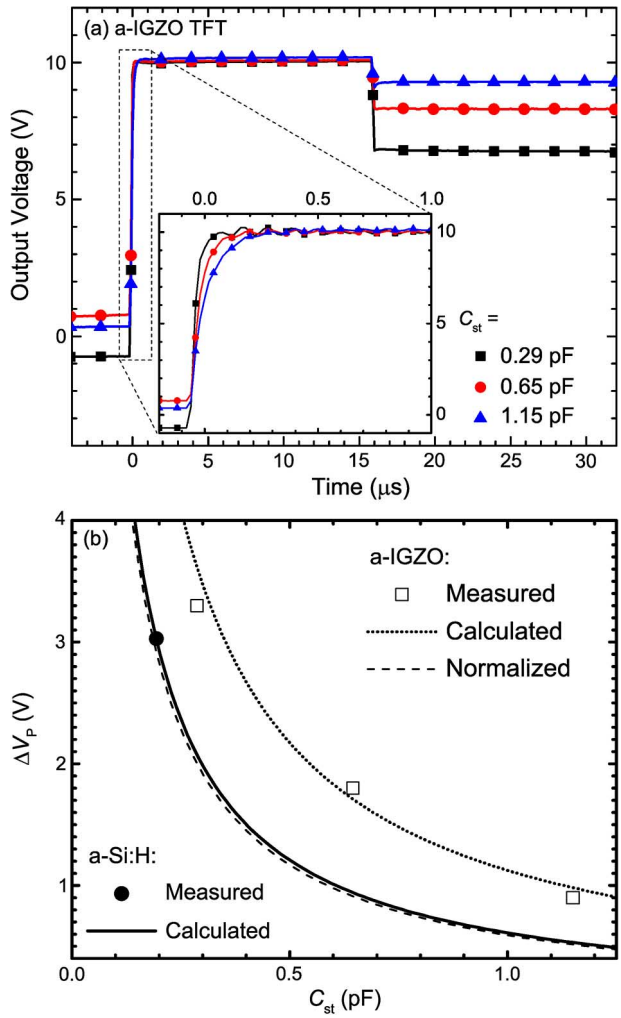

Fig. 10. (a) The $V_{\rm out}$ of a-IGZO TFT test circuits with different $C_{\rm st}$. The charging-time margin used for this figure is $t_{\rm cm} = 16$ μs. (b) The $\Delta V_{\rm P}$ for a-IGZO TFTs with different $C_{\rm st}$ extracted from (a) is shown as empty squares. The $\Delta V_{\rm P}$ is calculated using (9) and shown in the figure as dotted line ($\alpha = 0.32$). The normal a-Si:H TFT $\Delta V_{\rm P}$ is also shown in the figure as a solid circle, with the calculated values ($\alpha = 0.5$) represented as solid line. The same calculation is performed after normalizing the a-IGZO TFT for W, L, OVLP, and $C_{\rm GI}$ and shown as dashed line.

a-Si:H S/D contact regions remain unmodified even though the metal electrodes are recessed by 1/3.

To study the impact of $C_{\rm st}$ on the dynamic response of a-IGZO TFT test circuits, the output voltage for circuits with three different storage capacitances are characterized and shown in Fig. 10(a). The $t_{\rm FE}$ for the waveforms applied are all 10 ns. From the figure, we observe that larger $C_{\rm st}$ corresponds to higher charging times and lower $\Delta V_{\rm P}$, which is what we expect based on the previous analyses. The difference in terms of charging time is insignificant in this time-scale ($t_{\rm cm} = 16$ μs) and only observable in the Fig. 10(a) inset. Of particular interest is the $\Delta V_{\rm P}$, which we extract to be 3.3 V, 1.8 V, and 0.9 V for $C_{\rm st} = 0.29$, 0.65, and $1.15pF$, respectively, and shown in Fig. 10(b) as empty squares. The $\Delta V_{\rm P}$ for the normal a-Si:H TFT ($C_{\rm st} = 0.19$ pF) is extracted from Fig. 5 to be 2.71 V and is shown in the same figure as a solid circle. From (9), we calculate and show the relationship between $C_{\rm st}$ and $\Delta V_{\rm P}$ for a-Si:H (solid line) and a-IGZO TFTs (dotted line) in Fig. 10(b). We observe that because of device structure and geometry, the a-IGZO TFT has greater $\Delta V_{\rm P}$ than the a-Si:H TFT for the same $C_{\rm st}$. In Fig. 10(b), we normalize the a-IGZO TFT $\Delta V_{\rm P}$ curve based on the same geometry (W, L, OVLP) and $C_{\rm GI}$ as the a-Si:H TFT and show it as a dashed line. In the normalization of the a-IGZO TFT curve, we assume a-SiOx/a-SiNx bilayer gate insulator having the same $C_{\rm GI}$ as the 400-nm a-SiNx in a-Si:H TFT. We can thus conclude that given identical TFT geometries and structure, the a-IGZO TFT suffers no drawbacks to $\Delta V_{\rm P}$ and has vastly superior charging characteristics in comparison to the a-Si:H TFT. By implementing a larger $C_{\rm st}$, the $\Delta V_{\rm P}$ of a-IGZO TFTs can be further reduced. Increasing $C_{\rm st}$, as shown in Fig. 10(a), has negligible impact on the charging characteristics of the a-IGZO TFT. The limiting factor in this case would not be charging-time margin, but rather the aperture ratio of the AM-LCD pixel. This also bodes well for a-IGZO TFTs as the backplane technology of large-area AM-LCDs, which have larger liquid-crystal cells and thus greater cell capacitance.

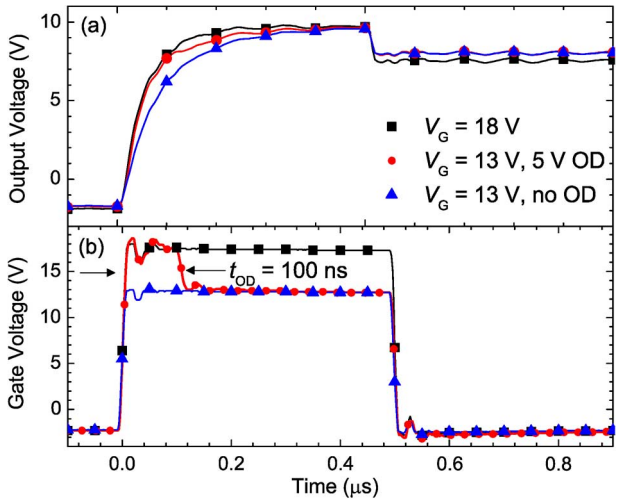

Fig. 11. The overdrive operation of the a-IGZO TFT in the test circle is shown in (a). The waveforms for baseline, overdrive, full overdrive is shown in (b). Overdrive operation adds $t_{\rm OD} = 100$ ns of $V_{\rm OD} = 5$ V on top of the baseline $V_{\rm GH} = 13$ V at the beginning of $t_{\rm cm}$. In full overdrive, the entire duration of $t_{\rm cm}$ is $V_{\rm GH} = 18$ V. For this experiment, test circuit with $C_{\rm st} = 0.65$ pF is evaluated.

C. a-IGZO TFT Gate Overdrive Operation

Overdrive operation was initially proposed for operation of individual AM-LCD cells to improve the gray-level response when displaying high-speed motion images [19]–[21]. Because there is a time delay in the gray-level transitions of a liquid crystal cell, the image signal can be pre-processed and an additional voltage (overdrive voltage $V_{\rm OD}$) can be added on top of the image signal to help the LC reach the desired transmittance faster. However, within published literature, the TFT has rarely been considered in the study of the overdrive method for AM-LCDs. In this work, we apply the voltage overdrive method to the gate signal of the a-IGZO TFT test circuit and the results are shown in Fig. 11 for $C_{\rm st} = 0.65$ pF. As shown in Fig. 11(b), three different gate waveforms are tested: $V_{\rm GH} = 18$ V (fully overdriven), $V_{\rm GH} = 13$ V+5 V (overdrive time $t_{\rm OD} = 100$ ns), and $V_{\rm GH} = 13$ V (baseline). Alternatively, we can also consider $V_{\rm GH} = 18$ V as the baseline, $V_{\rm GH} = 13$ V+5 V($t_{\rm OD} = 100$ ns) as partially underdriven, and $V_{\rm GH} = 13$ V as fully underdriven. In this scenario, by underdriving the TFT after the capacitor has been sufficiently charged, the final $V_{\rm GH}$ value is reduced, which according to (9) corresponds to lower $\Delta V_{\rm P}$. From Fig. 11(a), we see that the proposed method (solid circles) represents a good balance of both improved charging time compared to $V_{\rm GH} = 13$ V and lower $\Delta V_{\rm P}$ in comparison to $V_{\rm GH} = 18$ V. In our previous work, we have shown that reducing the duration of high gate voltage $(V_{\rm GH})$ in pulsed waveforms of a-IGZO TFT dynamic operation improves the ac bias-temperature stress (BTS) stability [18]. The partially underdriven method proposed in this study is expected to help reduce ac BTS instability and still retain adequate charging characteristics.

IV. Conclusion

To evaluate the dynamic response of a-Si:H and a-IGZO TFTs, we have fabricated test circuits in which a TFT is connected to a storage capacitor. For the a-Si:H TFT, in addition to the normal TFT configuration, we also fabricated the S/D-recessed TFT where the S/D metal is intentionally over-etched to reduce the gate-S/D overlap. Waveforms corresponding to UHD timing specifications are tested. Our results show that the S/D-recessed a-Si:H TFTs have slightly superior charging behavior and lower $\Delta V_{\rm P}$ compared to normal a-Si:H TFTs, but both are insufficient for 8 K × 4 K UHD AM-LCDs. Only the a-IGZO TFT is fully capable of supporting 8 K × 4 K resolution at 480 Hz.

Analytical expressions describing the feedthrough voltage $\Delta V_{\rm P}$ are investigated in detail. In particular, the impact of the gate signal falling edge $t_{\rm FE}$ is thoroughly studied. We find that for the short $t_{\rm FE}$ limit, channel charge redistribution and overlap capacitance feedthrough both contribute to $\Delta V_{\rm P}$. At the large-$t_{\rm FE}$ limit—approximately three orders of magnitude above the transit time—accumulated channel charges are almost completely released through the drain electrode and do not contribute to $\Delta V_{\rm P}$. In this case, $\Delta V_{\rm P}$ becomes entirely independent of $V_{\rm GH}$. The size of $C_{\rm st}$ is shown to have a strong impact on the $\Delta V_{\rm P}$ for a-IGZO TFTs, but has negligible influence on its charging behavior. After normalizing for TFT geometry and structure, $\Delta V_{\rm P}$ of a-IGZO TFTs is shown to be very similar to a-Si:H TFTs. Increasing the size of $C_{\rm st}$ can reduce the $\Delta V_{\rm P}$, and for a-IGZO TFTs this can be done without sacrificing charging behavior.

Lastly, we have demonstrated gate overdrive operation of the a-IGZO TFT by increasing the gate voltage beyond the pre-defined $V_{\rm GH}$ for a short interval within $t_{\rm cm}$. Our results show that overdrive operation allows for adequate charging of $C_{\rm st}$ while $\Delta V_{\rm P}$ is reduced. With its versatility and superior performance, the a-IGZO TFT is a very suitable backplane technology for large-area UHD AM-LCDs.

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